REMARKS

Applicant is in receipt of the Office Action mailed September 21, 2004. Claims 1-5 remain pending in the application.

35 U.S.C. § 103 Rejections

Claims 1-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Embree (U.S. Patent 6,104,222) in view of Adams (U.S. Patent 5,638,010). Applicant respectfully traverses the rejection.

Applicant notes that to establish a prima facie obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Applicant respectfully submits that even if the references cited were to be combined, the combination would not produce Applicant's invention as claimed in claims 1-5.

Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "the preconditioner receives a master clock signal, wherein the preconditioner outputs a modified clock signal that is synchronized to the master clock signal" and "the digital phase locked loop also receives the master clock signal, wherein the digital phase locked loop outputs an output clock signal, wherein the output clock signal is a version of the input clock signal synchronized to the master clock signal" as recited in independent claim 1. Embree fails to teach or suggest that the combination of elements 110, 120, 125, 130 and 140 receive "a master clock signal" as recited in claim 1 and that the PLL circuit 150 "also receives a master clock signal" as recited in claim 1. Embree further fails to teach or suggest that the output of VCO 130 (or the output element 140) and the output of PLL circuit 150 both are "synchronized to the master clock signal" as recited in claim 1. Additionally, Adams fails to teach or suggest "a preconditioner" as recited in claim 1, and Adams further fails to teach or

suggest that the output of "a preconditioner" and the output of the DPLL circuit 45 both are "synchronized to a master clock signal" as recited in claim 1.

Furthermore, Embree and Adams, whether alone or combined, fail to teach or suggest, "the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal" as recited in independent claim 1. The Examiner contends that this feature is implied in Column 1 Lines 58-65 of Embree. The Applicant respectfully disagrees with the Examiner's assertion. Embree teaches,

> "However, such an approach requires a substantially lengthy period for the PLL system 10 to lock onto the input clock signal, because the input clock signal operates at a low frequency, typically 24 Hz. In addition, the PLL system 10 is susceptible to noise conditions such as power supply fluctuations, etc. To avoid the slow response time and instability of such a PLL system, a higher input clock frequency is used." (Embree, Column 1, Lines 58-65)

The Applicant notes that the referenced section of the Embree patent highlights the shortcomings of the prior art by pointing out that the PLL system 10 is susceptible to noise conditions. Even if, for the sake of argument, one assumes that Embree and Adams teach a mechanism that reduces the noise conditions associated with a system, Embree and Adams, whether alone or combined, fail to teach or suggest "**the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal**" as recited in claim 1.

In accordance, claim 1 is believed to patentably distinguish over Embree and Adams, whether alone or combined. Claims 2-5 depend on claim 1 and are therefore believed to patentably distinguish over Embree and Adams, whether alone or combined, for at least the reasons given above.

Also, claim 2 recites, in part, "the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies; wherein the digital phase locked loop operates to remove the phase noise at the higher frequencies". The Examiner contends that this feature is taught in Column 1 Lines 58-65 of Embree. The Applicant notes that the referenced section (Column 1, Lines 58-65) of the Embree patent highlights the

shortcomings of the prior art by pointing out that the PLL system 10 is susceptible to noise conditions. The Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest "**the digital phase locked loop operates to remove the phase noise at the higher frequencies**" as recited in claim 2. In accordance, claim 2 is believed to patentably distinguish over Embree and Adams, whether alone or combined.

In addition, Applicant respectfully submits that Embree and Adams, whether alone or combined, fail to teach or suggest, "the preconditioner comprises...a latch having an input coupled to the output of the VCO, an input which receives the master clock signal, and including an output which generates the modified clock signal, wherein the latch synchronizes the modified clock signal to the master clock signal, wherein the output of the latch is coupled to the second input of the phase detector to provide the modified clock signal to the phase detector" as recited in claim 5. Applicant submits that Embree fails to teach or suggest element 140 having "an input which receives the master clock signal" as recited in claim 5, and Embree further fails to teach or suggest that element 140 "synchronizes" the output of the VCO 130 " to the master clock signal" as recited in claim 5. Also, as shown in Figure 2, Embree fails to teach or suggest that "the output" of element 140 "is coupled to" an "input of the phase detector" 120 as recited in claim 5. In addition, the Examiner contends that the highlighted features are taught by elements 70, 85, 87, and 88 on Figure 3 of Abrams. The Applicant respectfully submits that Figure 3 of Abrams fails to teach or suggest "a preconditioner" including the features highlighted above and coupled to a DPLL. Accordingly, claim 5 is believed to patentably distinguish over Embree and Adams, whether alone or combined.

CONCLUSION

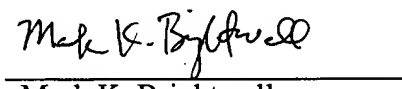
Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-47800/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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